REMARKS

Claims 29 and 33-35 remain in this application. Claims 30-32 have been canceled. Claim 29 has been amended twice, and claims 33-35 once.

Examiner S. Loke is thanked for having thoroughly examined the present invention.

A typographical error in amended drawing has been corrected to read (10). Hence, the reference numeral 10 on page 3 of the specification now appears in the amended Figure 1. It is believed that the examiner's objection has now been overcome, and it is so requested, respectfully.

Reconsideration of the rejection of claims 29 and 33-35 under 35 USC 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention is respectfully requested in view of the amendments and for the reasons given below.

Claim 29 has been amended to correct a typographical error citing "an oxide liner" to read "an oxide layer". The specification discloses an oxide layer, and hence it is believed that the rejection has now been overcome, and it is so requested, respectfully.

Reconsideration of the rejection of claims 34 and 35 under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, is respectfully requested in view of the amendments and for the reasons given below.

Claim 29 has been amended to cite both the "first conductive layer" and "the second conductive layer", which have the support in the specification on pages 15 and 19, respectively, as amended without new matter added. Hence, it is believed that claims 34 and 35 have the proper antecedent basis, and therefore are allowable, and it is so requested, respectfully.

Reconsideration of the rejection of claims 29-35 under 35 USC 103(a) as being unpatentable over Doan, et al., in view

of Sze is respectfully requested in view of the amendments and for the reasons given below.

The applicants are in agreement with the examiner that Doan, et al., disclose a stacked-gate flash memory. However, it is respectfully submitted that the stacked-gate flash memory of the instant invention differs from that of the primary reference because of the structural differences. Firstly, the referenced memory cells are constructed over field oxides, as differentiated from the trench oxides that the instant invention employs. The structure of a trench is different from field oxides, not only due to the depth of the trenches, but also because of the oxide lining layer the trenches have (page 14, lines 14-15 in the specification). Such oxide lining is lacking in the cited references. The trench isolations are also different because the trenches are filled with isolation oxide (please see page 17, line 16 of the specification), and not grown with field oxide as Doan, et al., disclose (column 3, line 61). Claim 29 has been amended to emphasize the depth of the instant trenches.

Furthermore, the high-step oxide used in the instant invention is likewise different structurally from a field oxide because of the height that can be formed with a filled

isolation oxide as a high-step oxide. This is clearly claimed in claim 29, lines 13-15, where the high-step oxide protrudes upward from the level of the opening of trench at the surface of the substrate reaching a height "s" 6000 Å even after chemical mechanical polishing (please see Fig. 3b and page 17, last paragraph flowing on to the next page 18). The applicant does indeed agree with the examiner that following the Sze formula, Doan, et al., can support an oxide height over the substrate not more than 3360 Å, because that is the limit of growing a field oxide. This is to be compared with almost double the height of the instant step-oxide above the surface of the substrate. That is the reason for depositing, in the instant invention, an isolation oxide into a trench that has been formed independent of an oxide field which can only be grown to a limited height out of silicon. Because of the exceptionally high high-step oxide, the inside walls of the opening that is formed in between the high-step oxide makes it possible to form a floating gate with tall folding surfaces to provide high coupling between the floating gate and the word line over the control gate, as can be seen in Fig. 3e. Such tall folding surfaces are totally lacking in the cited references.

It is respectfully suggested that the combination of these various references cannot be combined without reference to the applicants' own invention. None of the applied references address the problem of inadequate coupling ratio of conventional cells. Applicants have claimed their process in detail. The processes of Figs. 2a-2f and 3a-3g (Claims 29-35) are believed to be novel and patentable over these various references, because there is not sufficient basis for concluding that the combination of claimed elements would have been obvious to one skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable. We believe that there is no such basis for the combination. We therefore request respectfully that examiner S. Loke reconsider this rejection in view of these arguments and the amendments to the claims and allow claim 29 and claims dependent from claim 29.

Allowance of all claims, as amended, is requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. the attached page is captioned **"Version with Marking to Show Changes Made."**

It is requested that should the Examiner not find that the Claims Allowable that are now presented, that he call the undersigned Attorney at 845/452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE DRAWINGS

One replacement sheet marked in red for corrections for Fig. 1 is submitted for approval. Correction is made to one erroneously labeled reference numeral. No new matter added.

IN THE SPECIFICATION

On page 15, second paragraph has been amended as follows:

Next, floating gate oxide layer (160) is grown over the substrate, as shown in Fig. 2c. Subsequently, a first conductive [polysilicon] layer (170)- a polysilicon- later to be formed into a floating gate, is deposited over the gate oxide layer. Polysilicon is formed through methods including but not limited to Low Pressure Chemical Vapor Deposition (LPCVD) methods, Chemical Vapor Deposition (CVD) methods and Physical Vapor Deposition (PVD) sputtering

methods employing suitable silicon source materials. The floating gates are next defined by patterning a photoresist layer over the polysilicon layer and the floating gates formed by etching the first polysilicon layer exposed through the patterns in the photoresist layer, after which the photoresist layer is removed.

On page 19, second paragraph, has been amended as follows:

An interpoly oxide (280) is next formed over the contours of the conformal floating gate as shown in Fig. 3c. It is preferred that the interpoly oxide comprises oxide/nitride/oxide (ONO) formed through methods known in the art. Then, a second conductive [polysilicon] layer (290), a polysilicon, is formed over the interpoly oxide as shown both in the top view of the substrate in Fig. 3d, as well as the cross-sectional view, Fig. 3e. A third photoresist layer (not shown) is then used to form the control gate and word line (290) shown in Fig. 3e. A still another fourth photoresist layer (not shown) is used to define the self-aligned source (SAS) to form a common source line (200) shown in the top view of Fig. 3f. Thus, a stacked-gate as shown in the cross-sectional view of Fig. 3g, is formed.